CLAIMS

1. A method of fabricating a capacitor, comprising:
   forming a first electrode on a surface of a microfeature workpiece;
   forming a dielectric layer over the first electrode; and
   forming a second electrode over the dielectric layer;
   wherein at least one of the first electrode and the second electrode is formed by an electrode forming process including:
      reacting a first gaseous precursor and a second gaseous precursor to deposit a first electrically conductive layer at a first deposition rate; and
      depositing a second electrically conductive layer at a second deposition rate that is less than the first deposition rate by depositing a precursor layer of a third gaseous precursor at least one monolayer thick and exposing the precursor layer to a fourth gaseous precursor to form a nanolayer reaction product, the second electrically conductive layer being in contact with the dielectric layer and having a thickness of no greater than about 50Å.

2. The method of claim 1 wherein both the first precursor and the third precursor comprise a first chemical and both the second precursor and the fourth precursor comprise a second chemical .

3. The method of claim 1 wherein the surface of the microfeature workpiece includes a hemispherical grain polycrystalline silicon surface and forming the first electrode comprises depositing an electrically conductive coating on the hemispherical grain polycrystalline silicon surface.

4. The method of claim 1 wherein the nanolayer reaction product comprises a first nanolayer reaction product, and wherein forming the second electrically

conductive layer further comprises depositing a subsequent precursor layer of the third gaseous precursor at least one monolayer thick on the nanolayer reaction product and exposing the subsequent precursor layer to the fourth gaseous precursor to form a second nanolayer reaction product on the first nanolayer reaction product.

5. The method of claim 1 wherein the electrode forming process further comprises forming a third electrically conductive layer by depositing a precursor layer of the third gaseous precursor at least one monolayer thick and exposing the precursor layer to the fourth gaseous precursor to form another nanolayer reaction product, the first electrically conductive layer being disposed between the second electrically conductive layer and the third electrically conductive layer.

6. The method of claim 1 wherein the first and second electrically conductive layers are formed in a process chamber, depositing the precursor layer comprising introducing the third gaseous precursor to the process chamber and exposing the precursor layer comprises introducing the fourth gaseous precursor to the process chamber after introducing the third gaseous reactant.

7. The method of claim 6 further comprising purging the process chamber after forming the precursor layer and before exposing the precursor layer.

8. The method of claim 1 wherein the first electrode and the second electrode are each formed by the electrode forming process.

9. The method of claim 1 wherein the first electrode is formed by the electrode forming process and the first electrically conductive layer is formed before the second electrically conductive layer is formed, and wherein the precursor layer is deposited on the first electrically conductive layer, the dielectric layer

being formed by depositing a dielectric material on the second electrically conductive layer.

10. The method of claim 1 wherein the second electrode is formed by the electrode forming process and the second electrically conductive layer is formed before the first electrically conductive layer is formed, and wherein the precursor layer is deposited on the dielectric layer.

11. The method of claim 10 wherein the first electrically conductive layer is formed by depositing the first electrically conductive layer on the second electrically conductive layer.

12. The method of claim 1 wherein the second electrode is formed by the electrode forming process and the second electrically conductive layer is formed before the first electrically conductive layer is formed, and wherein the precursor layer is deposited on the dielectric layer.

13. The method of claim 1 wherein each of the first and third gaseous precursors comprises titanium and each of the second and fourth gaseous precursors comprises nitrogen, and wherein each of the first and second electrically conductive layers comprises titanium nitride.

14. The method of claim 13 wherein each of the first and third gaseous precursors comprises titanium chloride and each of the second and fourth gaseous precursors comprises ammonia.

15. A method of fabricating a microelectronic capacitor, comprising:
positioning a microfeature workpiece in a process chamber;
contemporaneously introducing a first gaseous precursor and a second gaseous precursor to the process chamber to deposit a first electrically conductive layer on a surface of the microfeature workpiece;

thereafter, terminating introduction of at least one of the first and second gaseous precursors and alternately introducing a quantity of the first gaseous precursor and a quantity of the second gaseous precursor to the process chamber to form a second electrically conductive layer at a location spaced outwardly from the surface of the microfeature workpiece, the second electrically conductive layer having a thickness of no greater than 50Å;

forming a dielectric layer on the second electrically conductive layer; and

forming an electrically conductive electrode on the dielectric layer.

16. The method of claim 15 further comprising purging the process chamber after introducing the quantity of the first gaseous precursor and before introducing the quantity of the second gaseous precursor.

17. The method of claim 15 further comprising depositing at least one additional electrically conductive layer between the first electrically conductive layer and the second electrically conductive layer.

18. The method of claim 15 further comprising, after depositing the first electrically conductive layer and before depositing the second electrically conductive layer:

depositing a third electrically conductive layer on the first electrically conductive layer by sequentially introducing quantities of the first gaseous precursor and quantities of the second gaseous precursor to the process chamber; and

depositing a fourth electrically conductive layer on the third electrically conductive layer by contemporaneously introducing the first gaseous precursor and the second gaseous precursor to the process chamber.

19. The method of claim 15 wherein the surface of the microfeature workpiece includes a hemispherical grain polycrystalline silicon surface and the first

electrically conductive layer is deposited on the hemispherical grain polycrystalline silicon surface.

20. The method of claim 15 wherein forming the electrically conductive electrode comprises introducing the first gaseous precursor and the second gaseous precursor to the process chamber at the same time.

21. The method of claim 15 wherein forming the electrically conductive electrode comprises:

sequentially introducing quantities of the first gaseous precursor and quantities of the second gaseous precursor to the process chamber to form a first electrode layer having a thickness of no greater than 50Å; and

introducing the first gaseous precursor and the second gaseous precursor to the process chamber at the same time to deposit a second electrode layer on the first electrode layer.

22. The method of claim 15 wherein the first gaseous precursor comprises titanium and the second gaseous precursor comprises nitrogen, and wherein each of the first and second electrically conductive layers comprises titanium nitride.

23. A method of fabricating a microelectronic capacitor, comprising:

positioning a microfeature workpiece in a process chamber;

alternately introducing a quantity of a first gaseous precursor and a quantity of a second gaseous precursor to the process chamber to form a first electrically conductive layer on a surface of the microfeature workpiece, the first electrically conductive layer having a thickness of no greater than 50Å;

thereafter, contemporaneously introducing the first gaseous precursor and the second gaseous precursor to the process chamber to deposit a second

electrically conductive layer at a location spaced outwardly from the surface of the microfeature workpiece;

forming a dielectric layer on the second electrically conductive layer; and

forming an electrically conductive electrode on the dielectric layer.

24. The method of claim 23 further comprising purging the process chamber after introducing the quantity of the first gaseous precursor and before introducing the quantity of the second gaseous precursor.

25. The method of claim 23 further comprising depositing at least one additional electrically conductive layer between the first electrically conductive layer and the second electrically conductive layer.

26. The method of claim 23 further comprising, after depositing the first electrically conductive layer and before depositing the second electrically conductive layer:

depositing a third electrically conductive layer on the first electrically conductive layer by contemporaneously introducing the first gaseous precursor and the second gaseous precursor to the process chamber; and

depositing a fourth electrically conductive layer on the third electrically conductive layer by sequentially introducing quantities of the first gaseous precursor and quantities of the second gaseous precursor to the process chamber.

27. The method of claim 23 wherein the surface of the microfeature workpiece includes a hemispherical grain polycrystalline silicon surface and the first electrically conductive layer is deposited on the hemispherical grain polycrystalline silicon surface.

28. The method of claim 23 wherein forming the electrically conductive electrode comprises introducing the first gaseous precursor and the second gaseous precursor to the process chamber at the same time.

29. The method of claim 23 wherein forming the electrically conductive electrode comprises:

sequentially introducing quantities of the first gaseous precursor and quantities of the second gaseous precursor to the process chamber to form a first electrode layer having a thickness of no greater than 50Å; and

introducing the first gaseous precursor and the second gaseous precursor to the process chamber at the same time to deposit a second electrode layer on the first electrode layer.

30. The method of claim 23 wherein the first gaseous precursor comprises titanium and the second gaseous precursor comprises nitrogen, and wherein each of the first and second electrically conductive layers comprises titanium nitride.

31. A method of fabricating a microelectronic capacitor, comprising:

positioning a microfeature workpiece in a process chamber;

forming an electrode on a surface of the microfeature workpiece;

forming a dielectric layer on the electrode;

alternately introducing a quantity of a first gaseous precursor and a quantity of a second gaseous precursor to the process chamber to form a first electrically conductive layer on the dielectric layer, the first electrically conductive layer having a thickness of no greater than 50Å; and

contemporaneously introducing the first gaseous precursor and the second gaseous precursor to the process chamber to deposit a second electrically conductive layer at a location spaced from the dielectric layer.

32. The method of claim 31 further comprising purging the process chamber after introducing the quantity of the first gaseous precursor and before introducing the quantity of the second gaseous precursor.

33. The method of claim 31 further comprising depositing at least one additional electrically conductive layer between the first electrically conductive layer and the second electrically conductive layer.

34. The method of claim 31 further comprising, after depositing the first electrically conductive layer and before depositing the second electrically conductive layer:

depositing a third electrically conductive layer on the first electrically conductive layer by contemporaneously introducing the first gaseous precursor and the second gaseous precursor to the process chamber; and

depositing a fourth electrically conductive layer on the third electrically conductive layer by alternately introducing a quantity of the first gaseous precursor and a quantity of the second gaseous precursor to the process chamber.

35. The method of claim 31 wherein forming the electrode comprises forming a layer of hemispherical grain polycrystalline silicon.

36. The method of claim 31 wherein forming the electrode comprises contemporaneously introducing the first gaseous precursor and the second gaseous precursor to the process chamber.

37. The method of claim 31 wherein forming the electrode comprises:

contemporaneously introducing the first gaseous precursor and the second gaseous precursor to the process chamber to deposit a first electrode; and

sequentially introducing quantities of the first gaseous precursor and quantities of the second gaseous precursor to the process chamber to deposit a second electrode layer having a thickness of no greater than 50Å layer on the first electrode layer.

38. The method of claim 31 wherein the first gaseous precursor comprises titanium and the second gaseous precursor comprises nitrogen, and wherein each of the first and second electrically conductive layers comprises titanium nitride.

39. A method of fabricating a microelectronic capacitor electrode, comprising:
positioning a microfeature workpiece in a process chamber;
forming an electrically conductive structure on a surface of the microfeature workpiece by:
depositing a first electrically conductive layer by a first deposition process comprising contemporaneously introducing a first gaseous precursor and a second gaseous precursor to the process chamber to form a first reaction product of the first and second precursors;
depositing a second electrically conductive layer on the first electrically conductive layer by a second deposition process comprising alternately introducing quantities of the first gaseous precursor and quantities of the second gaseous precursor to the process chamber to form at least two layers of a second reaction product of the first and second precursors, the second reaction product having a lower impurity content than the first reaction product;
depositing a third electrically conductive layer on the second electrically conductive layer by the first deposition process; and
depositing a fourth electrically conductive layer on the third electrically conductive layer by the second deposition process.

40. A method of fabricating a microelectronic capacitor, comprising:

depositing a first conductive layer at a first rate by reacting a first gaseous precursor and a second gaseous precursor in a first reaction process, the first conductive layer having a first surface roughness and a first impurity content;

depositing a second conductive layer at a second rate, which is slower than the first rate, by reacting the first gaseous precursor and the second gaseous precursor in a second reaction process, the second conductive layer having a second surface roughness that is smoother than the first surface roughness and a second impurity content that is lower than the first impurity content;

thereafter, depositing a dielectric layer; and

depositing an electrode on the dielectric layer.

41. The method of claim 40 wherein the first reaction process comprises chemical vapor deposition.

42. The method of claim 40 wherein the first reaction process comprises chemical vapor deposition and the second reaction process comprises atomic layer deposition.

43. The method of claim 40 wherein the first gaseous precursor comprises titanium and the second gaseous precursor comprises nitrogen, and wherein each of the first and second electrically conductive layers comprises titanium nitride.

44. The method of claim 40 wherein the first gaseous precursor comprises titanium chloride and the second gaseous precursor comprises ammonia, and wherein the first impurity level comprises a concentration of chlorine and the second impurity level comprises a lower concentration of chlorine.

45. A microelectronic component comprising a plurality of memory cells carried by a substrate, each memory cell including a capacitor comprising:

a first electrode including, moving outwardly from a surface of the substrate, a hemispherical grain polycrystalline silicon layer, a layer of a bulk deposition product comprising a primary species, and a layer of a nanolayer deposition product comprising the same primary species, the layer of the nanolayer deposition product having a thickness of no greater than 50Å and the bulk deposition product having an impurity content higher than an impurity content of the nanolayer deposition product;

a dielectric layer deposited on the nanolayer deposition product of the first electrode; and

a second electrode deposited on the dielectric layer.

46. The microelectronic component of claim 45 wherein the layer of the bulk deposition product has a first interface surface oriented away from the substrate and the layer of the nanolayer deposition product has a second interface surface oriented away from the substrate and in contact with the dielectric layer, the first interface surface having a surface roughness greater than a surface roughness of the second interface surface.

47. A microfeature workpiece processing system comprising:

an enclosure defining a process chamber adapted to receive a microfeature workpiece;

a gas supply adapted to selectively deliver a first gaseous precursor, a second gaseous precursor, and a third gaseous precursor to the process chamber; and

a programmable controller operatively coupled to the gas supply, the controller being programmed to:

contemporaneously introduce the first gaseous precursor and the second gaseous precursor from the gas supply to the process chamber to

deposit a first electrically conductive layer on a surface of the microfeature workpiece;

terminate introduction of at least one of the first and second gaseous precursors;

alternately introduce a quantity of the first gaseous precursor and a quantity of the second gaseous precursor from the gas supply to the process chamber to form a second electrically conductive layer at a location spaced outwardly from the surface of the microfeature workpiece, the second electrically conductive layer having a thickness of no greater than 50Å; and

thereafter, introduce the third gaseous precursor to the process chamber to form a dielectric layer on the second electrically conductive layer.

48. The microfeature workpiece processing system of claim 47 wherein the gas supply is further adapted to deliver a purge gas and the controller is further programmed to purge the process chamber with the purge gas after introducing the quantity of the first gaseous precursor and before introducing the quantity of the second gaseous precursor.

49. The microfeature workpiece processing system of claim 47 wherein the first gaseous precursor comprises titanium and the second gaseous precursor comprises nitrogen.